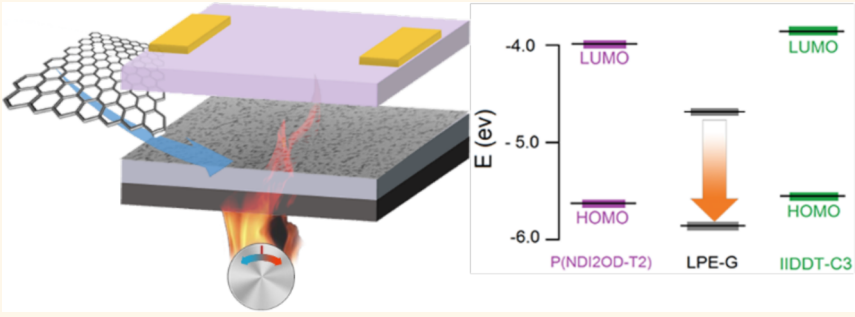
A Multifunctional Polymer-Graphene Thin-Film Transistor with Tunable Transport Regimes

Thomas Mosciatti,[†] Sébastien Haar,[†] Fabiola Liscio,[‡] Artur Ciesielski,[†] Emanuele Orgiu,[*,†] and Paolo Samori[*,†]

[†]ISIS & icFRC, Université de Strasbourg & CNRS, 8 allée Gaspard Monge, 67000 Strasbourg, France and [‡]Istituto per la Microelettronica e Microsistemi (IMM) — CNR, via Gobetti 101, 40129 Bologna, Italy

ABSTRACT



Here we describe a strategy to fabricate multifunctional graphene-polymer hybrid thin-film transistors (PG-TFT) whose transport properties are tunable by varying the deposition conditions of liquid-phase exfoliated graphene (LPE-G) dispersions onto a dielectric surface and *via* thermal annealing post-treatments. In particular, the ionization energy (IE) of the LPE-G drop-cast on SiO_2 can be finely adjusted prior to polymer deposition *via* thermal annealing in air environment, exhibiting values gradually changing from 4.8 eV up to 5.7 eV. Such a tunable graphene's IE determines dramatically different electronic interactions between the LPE-G and the semiconducting polymer (*p*- or *n*-type) sitting on its top, leading to devices where the output current of the PG-TFT can be operated from being completely turned off up to modulable. In fact upon increasing the surface coverage of graphene nanoflakes on the SiO_2 the charge transport properties within the top polymer layer are modified from being semiconducting up to truly conductive (graphite-like). Significantly, when the IE of LPE-G is outside the polymer band gap, the PG-TFT can operate as a multifunctional three terminal switch (transistor) and/or memory device featuring high number of erase-write cycles. Our PG-TFT, based on a fine energy level engineering, represents a memory device operating without the need of a dielectric layer separating a floating gate from the active channel.

KEYWORDS: graphene · organic thin-film transistor · memory device · hybrid material · multifunctionality

The modern electronics industry is continuously searching for novel materials and processing methods that could lead to devices based on new physical concepts, paving the way toward the exploitation of unprecedented properties. Among these novel materials, graphene has certainly garnered a great deal of attention. Graphene is constituted by a single layer of covalently tethered carbon atoms arranged in a honeycomb lattice; it is a zero band gap semiconductor exhibiting extraordinary electronic properties.[1,2] To become a golden component for the electronic industry, two greatest challenges need to be addressed: (i) developing methods that can be up-scaled for mass production of high quality graphene, and (ii) opening a band gap to "switch off" graphene devices and thus make them suitable for logic application.[3,4] On the one hand, liquid-phase exfoliation of graphite into graphene is emerging as a suitable up-scalable method for the production of high quality graphene.[5−9] On the other hand, different strategies have been proposed in order to open a band gap in graphene such as the production of reduced graphene oxide[10,11] or graphene nanoribbons.[12−16] A different way of employing graphene for electronics relies on the use of hybrid solutions that combine graphene with

* Address correspondence to samori@unistra.fr, orgiu@unistra.fr.

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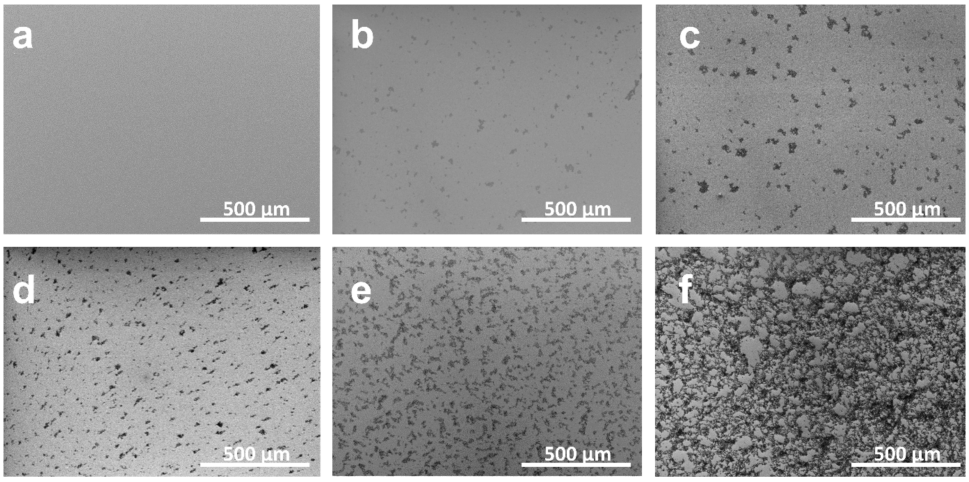

Figure 1. SEM images of LPE-G patterns on SiO_2 obtained by applying to the dielectric surfaces dispersions in NMP with increasing volume after thermal annealing at 415 °C for 14 h. (a) no graphene, (b) 2.5 μL, (c) 5 μL, (d) 10 μL, (e) 15 μL, (f) 20 μL.

suitable molecules to enable reciprocal modification of the component properties, *e.g.*, *via* tailoring of interfaces or blending. Graphene/inorganic devices were proposed for different ferroelectric and semiconductors applications[17] or as excellent option for radio frequency transistors that do not need high I_{on}/I_{off} ratio.[18] Liquid-phase exfoliated graphene (LPE-G) in the presence of suitable molecules was successfully used as a bicomponent graphene/organic hybrid active layer for tuning the transport in thin-film transistors.[19,20] A well explored way to address this approach relies on the use of a blend of graphene and an organic or polymeric semiconductor, although blends exhibit mayor downsides like phase segregation,[19] graphene random aggregation,[21] crystallinity loss in the semiconductor matrix[22] and very poor control over graphene deposition.[23]

Here we describe a novel strategy for fabricating a multifunctional polymeric-graphene thin-film transistor (PG-TFT) that relies on solution processing of semiconducting polymers on the top of solution processed graphene nanoscale patches having thermally tunable IE. This graphene's energy level engineering resulting in a broad range of IEs makes it possible to modulate the electronic interactions between the LPE-G and the semiconducting polymer. In this work, we focused our attention on two exemplary cases, *i.e.*, LPE-G with an IE laying either inside or outside the band gap of either a *p*- or an *n*-type polymer active layer. When the IE is outside the polymer band gap one obtains tunable device's working regimes, which depend on the surface coverage. In particular, it was possible to adjust the transport in the bicomponent film from semiconducting to truly conductive, *i.e.*, exhibiting no gate modulation. The control over the IE of deposited LPE-G interacting with the polymer makes it possible also to operate the three-terminal device as a memory element without the need of depositing a further dielectric interlayer as previously reported in literature.[24−26] Noteworthy, the approach has been tested with both *n*- and *p*-type polymer semiconductor demonstrating that this novel and general working mechanism is viable for both hole and electron transport.

RESULTS AND DISCUSSION

The device fabrication started with controlled deposition of LPE-G dispersion on SiO_2. The exfoliated graphene dispersion contains high-quality graphene with a concentration of mono and bilayer flakes exceeding 55%, as reported in our previous study.[5] A variable volume (nominally 2.5, 5, 10, or 20 μL) of LPE-G dispersion was drop-cast on the SiO_2 surface. The obtained samples were thermally annealed at 415 °C. The scanning electron microscope (SEM) images in Figure 1 display the morphology of films obtained by drop-casting an increasingly greater volume of LPE-G on the SiO_2 surface, followed by thermal annealing. It reveals an increase in surface coverage (amounting to 2.5, 5.5, 12.5, 20, and 50%) with isolated graphene nanopatches merging to form a continuous network. Importantly, for each specific volume employed, the coverage of the graphene pattern is homogeneous over the whole sample surface.

The thermal annealing treatments of the LPE-G dispersion drop-cast on the SiO_2 were carried out at 415 °C either in environmental conditions, *i.e.*, at RT and RH = 20−30%, or in a nitrogen-filled atmosphere, *i.e.*, with a few ppm of oxygen and water, in order to remove the *N*-methylpyrrolidone (NMP) solvent leftover, including interflake residues as proved by X-ray photoelectron spectroscopy (XPS) (see Supporting Information (SI)). In the former case, the IE of graphene patches annealed in air was found to shift from 5.0 to 5.7 eV with an exponential trend reaching a plateau after 4 h as shown in Figure 2c where the average value (with standard deviation) obtained from two set of samples is reported for each different

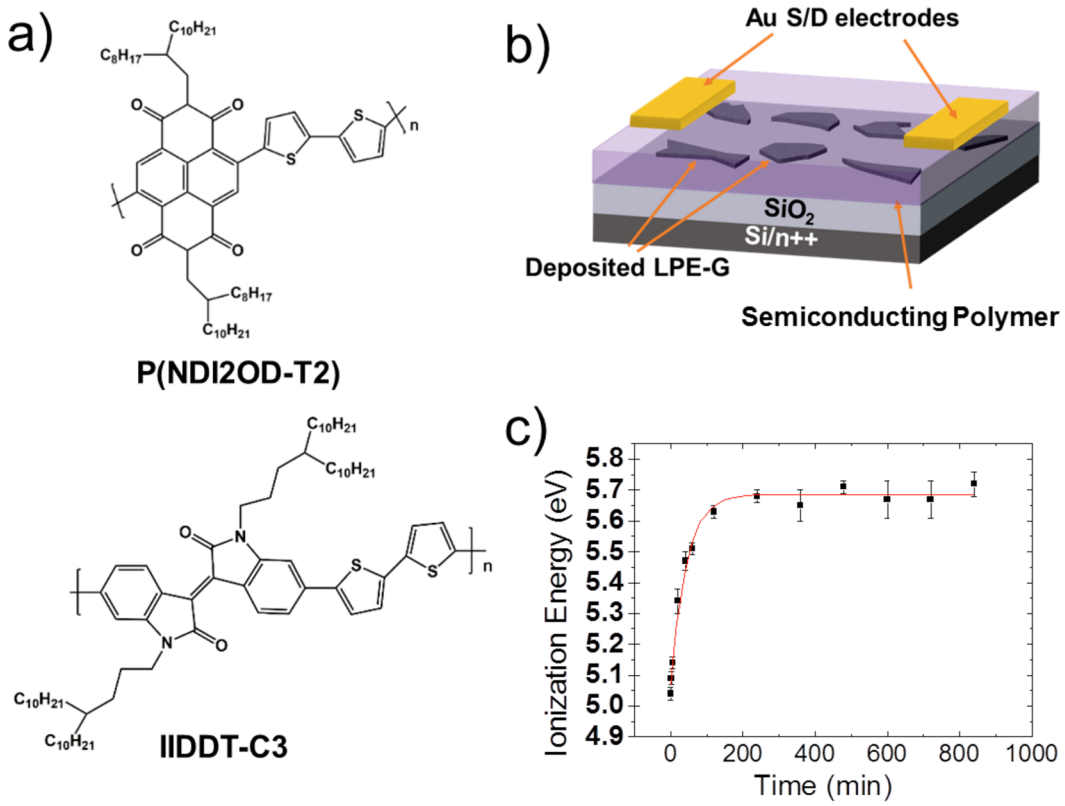

Figure 2. (a) Chemical formula of the two polymeric semiconductors encompassed in this study. (b) Scheme of the device geometry implemented, showing the deposition of LPE-G on the SiO_2 dielectric surface, the polymer thin film and the top gold electrodes. (c) Average ionization energy shift measured by ambient photoelectron spectroscopy at different annealing time (at 415 °C in air environment) and the single exponential fitting thereof. Error bars are the measurement's standard deviation.

annealing time. In the latter case, when the LPE-G deposited on SiO_2 is annealed under N_2 atmosphere at 415 °C for 14 h the IE value was found to remain constant at 4.9 eV. The possibility of modulating the IE made it possible to explore the electronic interaction between a polymeric semiconductor and the graphene with IE values at their two extremes, thereby placing the IE level either outside or inside the semiconductor band gap.

By taking advantage of the insoluble nature of the thermally annealed LPE-G patches, prior to the deposition of the polymer layer a further functionalization from solution of the SiO_2 areas uncoated by the graphene with octadecyltrichlorosilane (OTS) were carried out in order to render them more hydrophobic. In essence, such a treatment has the ultimate goal of promoting crystallization of the semiconducting polymer in thin continuous film as well as preventing the electron trapping coming from the silanol groups at the surface.[27] A 60 nm thick polymer semiconductor film (measured with a profilometer) was spin-coated onto the LPE-G prepatterned on SiO_2. The fabrication of the OTFT was completed with thermal evaporation of two gold top pads acting as the source and drain electrodes (Figure 2b). As polymer semiconductor we focused our attention on a *n*-type polymer, *i.e.*, poly[*N*,*N*-9-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-*alt*-5,59-(2,29-bithiophene)], P(NDI2OD-T2) (purchased from Polyera Corporation), and a *p*-type polymer, *i.e.*, poly[1,1′-bis(4-decyltetradecyl)-6-methyl-6′-(5′-methyl-[2,2′-bithiophen]-5-yl)-[3,3′-biindolinylidene]-2,2′-dione] IIDDT-C3 (purchased from 1-Materials Inc.) which were used as the active layers in the TFT devices (Figure 2a). Both polymers combine high charge carrier mobility, air-stability and HOMO/LUMO levels close in energy, as revealed by cyclic voltammetry.[28,29]

Figure 3a,b display the energy diagrams which include the polymer's HOMO and LUMO levels as well as the respective IE of LPE-G annealed in a given environment. When LPE-G was annealed under N_2 atmosphere the IE amounts to 4.9 eV, which implies that this level lies inside the band gap of both polymers, thereby allowing graphene to act as (deep) trap center in the channel. Thermal annealing of LPE-G at 415 °C for 4 h in air environment, lead to a drastic change in IE value which shifts to 5.7 eV (see SI for analysis). Such a value falls outside both polymers' band gap, thus in such a case the LPE-G cannot act as an energy trap for charges. Overall, the IE of the deposited LPE-G can be modified by changing the duration of thermal annealing at 415 °C and the

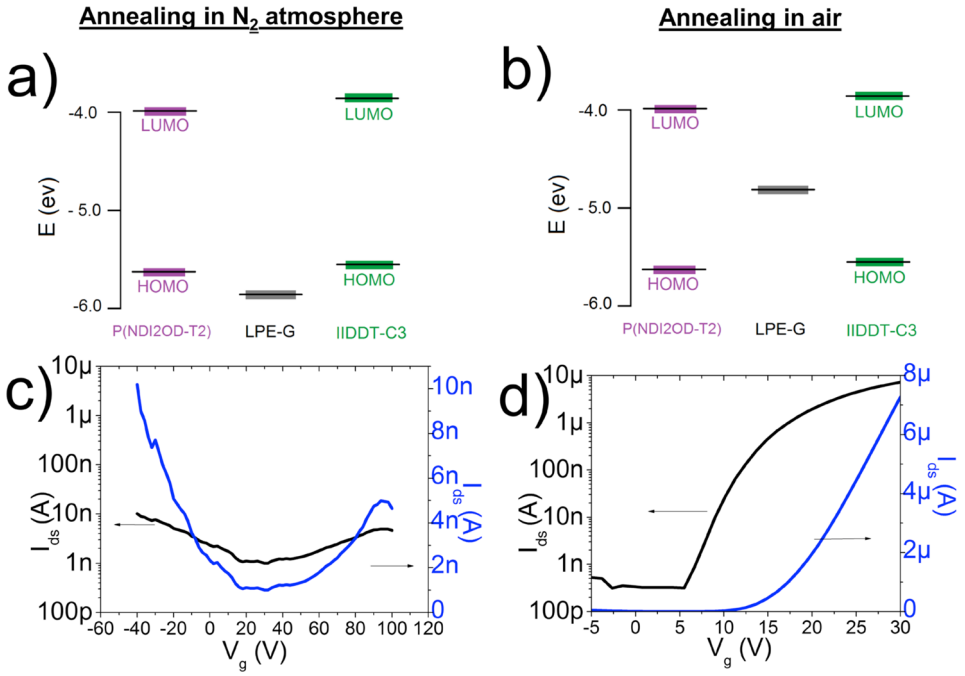

Figure 3. Energy scheme of LPE-G, with respect to the two polymeric semiconductors HOMO/LUMO levels as measured by ambient photoelectron spectroscopy (see SI), annealed at 415 °C for 15 h (a) under nitrogen, and (b) in ambient conditions. (c) Transfer characteristic of a typical P(NDI2OD-T2) device with 10 μL of LPE-G deposited on the gate annealed under nitrogen. (d) Transfer characteristic of a typical P(NDI2OD-T2) device with 10 μL of LPE-G deposited on the gate annealed in ambient conditions. The current is reported in the same logarithmic scale (black) to underline the different conduction properties of the two systems.

environment in which such an annealing is executed. Figure 3c,d portrays the transfer characteristics of device consisting of P(NDI2OD-T2) spin-coated on LPE-G that was previously drop-cast on SiO_2 (volume = 10 μL) and annealed at 415 °C for 15 h either under N_2 atmosphere or in air, respectively. Figure 1c reveals a drastic reduction in both the output current of the device and in the gate modulation effect. In particular, currents below 10 nA were measured together with very low gate modulation. On the other hand, when the ionization energy of LPE-G is higher in energy than the HOMO of both polymers (Figure 1d), the TFTs exhibit a very good behavior with current exceeding 10 μA and high mobility values (full comparison for both polymer with the two different energetic scheme are reported in the SI). In light of these findings we decided to perform an in-depth study of devices based on LPE-G drop-cast on SiO_2 followed by thermal annealing in air environment.

The LPE-G nanopatches on SiO_2 shown in Figure 1, exhibiting different coverages, were used as templates for the fabrication of hybrid graphene-polymer based TFTs. In particular, the effect of degree of coverage of graphene nanopatches on SiO_2 on the charge transport in the hybrid material was explored by fabricating bottom-gate top-contact TFTs using the two semiconducting polymers described above.

Smooth polymer films (Figure S9a, S10a) were prepared by spin-coating onto the previously patterned LPE-G samples (Figure 4a) followed by the evaporation of the gold top electrodes. These PG-TFTs were characterized in order to cast light onto the role of the graphene nanopatches annealed in air on the electrical properties of the hybrid active layer, by quantifying the relevant device parameters such as the field-effect mobility, threshold voltage and I_{on}/I_{off} ratio. We prepared two set of samples for each polymer. This allowed us to measure 16 devices for each different surface coverage for a total of 80 devices for each polymer. As a general trend, the device output current increased with the degree of coverage of graphene on the surface, but such an enhancement is accompanied by different changes in electrical performances (Figure 4b). Four different types of device operation could be identified based on our data. (I) Semiconducting behavior ($I_{on}/I_{off} > 10^5$, strong gate field-effect); (II) enhanced semiconducting behavior ($I_{on}/I_{off} \sim 10^5-10^4$, strong gate field-effect, increase in mobility); (III) semiconducting/graphene hybrid behavior ($I_{on}/I_{off} < 10^3$, low gate field-effect, OFF currents $>10^{-7}$ A); (IV) graphene-like behavior ($I_{on}/I_{off} < 10$, no gate field-effect, current $>10^{-4}$ A). When 0−5 μL of LPE-G were drop-cast on the dielectric surface, an increase in the recorded current and field-effect mobility for both polymers was observed entering in regime (II). In particular, compared to the pristine devices (I), the graphene prepatterned based TFT incorporating P(NDI2OD-T2) and IIDDT-C3 exhibited an over ten- and 3-fold increase in field-effect mobility, respectively. This improved mobility is attained at the expenses of a subtle decrease of the I_{on}/I_{off} ratio (being below 1 order of magnitude),

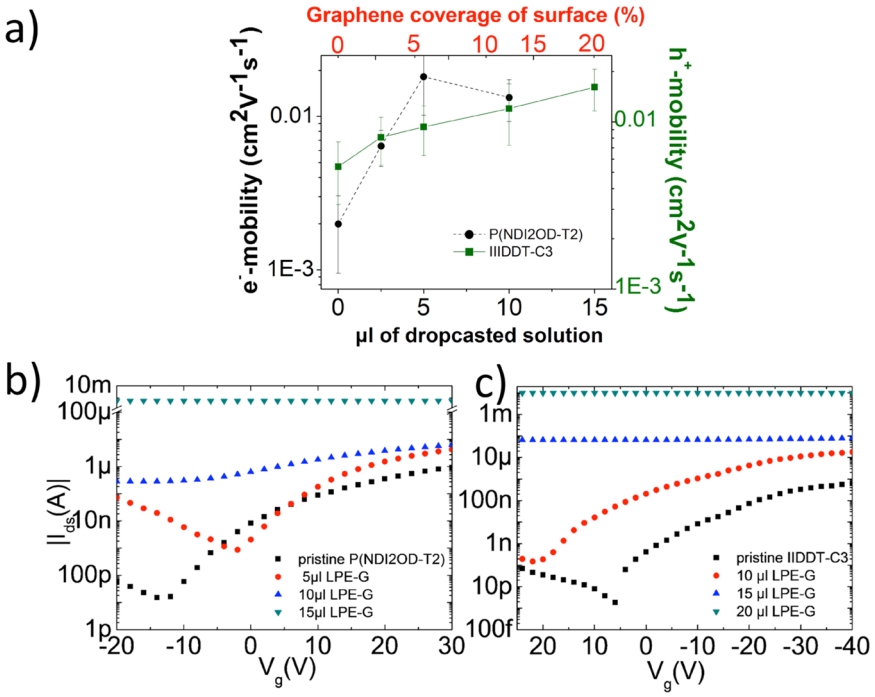

Figure 4. (a) Average field-effect mobility for P(NDI2OD-T2) and IIDDT-C3 films supported on prepatterned LPE-G at increasing volume of LPE-G suspension deposited on SiO_2 surface (bottom axis) and respective LPE-G surface coverage (top axis) (error bars correspond to standard deviation). (b) Transfer characteristic of devices for different amounts of LPE-G deposited on the gate surface for P(NDI2OD-T2) and (c) IIDDT-C3 based devices. The curves displayed are representative of the 4 working, *i.e.*, conductive, regimes found in the system. Channel length 100 μm, channel width 10 000 μm, V_{ds} = 40 V for P(NDI2OD-T2) and V_{ds} = −40 V for IIDDT-C3.

indicating a preponderant semiconducting working regime. Upon increasing the graphene deposited on the surface, by drop-casting 10−15 μL LPE-G on the SiO_2, hybrid (III) or graphenic (IV) devices were obtained. In hybrid devices gate modulation is still present, but the I_{on}/I_{off} ratio is reduced significantly with respect of regime (II) most likely indicating that LPE-G on the gate surface is enough interconnected to generate partial percolation pathways. This proves that the graphene effect on I_{on}/I_{off} ratio is related to gate voltage modulation, which decreases up its disappearance when a fully interconnected network of deposited graphene acts as a percolation pathways for charges. In this regime (IV), because of the high amount of graphene adsorbed on SiO_2, the devices display a drastic reduction of I_{on}/I_{off} ratio. In general, the I_{on}/I_{off} ratio decreases progressively upon increasing the graphene content in the device (Figure 4b,c). The graphene-like regime displays high current and no gate modulation in logarithmic scale, while a small but measurable gate effect is still evident in Figure S6d and S7d. This is in accordance with our previous measurements[5] on LPE-G-based devices treated with the same annealing process as in the present work. As a result of the thermal treatment the deposited LPE-G on SiO_2 can electronically behave as graphene, in particular the presence of Dirac point and high current flowing, providing evidence for absence of a chemical oxidation of graphene induced despite thermal annealing treatment. Interestingly, the transition between semiconducting to fully graphenic transport regime is not abrupt but it can be finely tuned upon changing the degree of coverage of the graphene nanopatches prepatterning the surface. The mobility increase is strongly correlated with the degree of coverage of the LPE-G pattern on the dielectric gate surface up to a point in which devices cannot be turned off, albeit preserving gate modulation. Those two intermediate regimes are particularly interesting from a scientific and engineering point of view. In fact, having a regime in which mobility is enhanced with an I_{on}/I_{off} ratio exceeding 10^5 and a regime in which we can have higher current flowing yet still gate effect modulation open future possibilities on the application of this method for fabricating tunable graphene/organic hybrid device.

To gain a greater understanding on the enhanced electrical characteristics in the enhanced semiconducting regime (II) and in general on the effect of the prepatterning of the SiO_2 with graphene when a polymer is spin-coated on its top, we explored the structure and morphology of the graphene and graphene/polymer films. Grazing incidence X-ray diffraction (2D-GIXRD) measurements executed on films with different combinations of polymer *vs* LPE-G surface coverage provided evidence for the absence of significant structural differences in the polymer crystallinity upon increasing the content of LPE-G coating the SiO_2 surface (see SI). Atomic force microscopy (AFM)

studies on the graphene nanopatches on SiO_2 and the bicomponent graphene/polymer films revealed that the roughness of prepatterned LPE-G nanopatches (Figure S3, S4) is partially transferred to the top polymer film. While monocomponent polymer films are very smooth, as evidenced by a root-mean-square roughness (R_{rms}) below 1 nm determined on a 25 μm^2 AFM image, the presence of underlying LPE-G generates 6 nm thick ripples on the polymer film surfaces when 10 μL of LPE-G are deposited as reported in Figure S5. Nevertheless, the polymer crystallites are still visible (Figure S9 and Figure S10).

Those findings are instrumental to correlate hybrid and graphenic regimes to graphene surface coverage on SiO_2. When spatially extended aggregates of deposited graphene are placed directly under evaporated source and drain gold electrodes they can form a continuous path through the channel, hence a graphenic device regime is obtained. For less continuous network of graphene the percolation path is interrupted, thus the charges are forced to travel through polymeric layer, allowing for partial yet evident gate modulation (hybrid regime). In view of the unaltered crystallinity within the polymer film as observed by 2D-GIXRD, the enhancement in mobility in the devices can be ascribed to electronic/electrostatic interaction between graphene and polymer. Since we used LPE-G patches thermally annealed in air environment, thereby having an IE = 5.7 eV, the interactions between graphene and semiconductors can solely be of electrostatic nature. Our system with a layer (*i.e.*, LPE-G) whose IE is sitting off the polymer band gap can thus be related to works where graphene and reduced graphene oxide has been extensively studied as floating gate,[30] to build memories[31,32] and nanomemories.[33] Since continuous films (or aggregates forming continuous percolation pathways) of graphene nanoflakes behave as a semimetallic material[34] our system can also be benchmarked to works where deposited metallic nanoparticles on a surface were proved to act as floating gate[25,35,36] and to be suitable for building memory device.[37] The above-mentioned approaches require the use of a dielectric layer between the nanoparticles and the active material, because direct contact between them would generate charge trapping and give raise to nonfunctioning devices.[38,39] This scenario is equivalent in our case when using LPE-G patches with an IE within the band gap, thereby generating states that act as traps or recombination centers for charges, which are extremely efficient in decreasing the overall device performance, as reported for system using metallic nanoparticles on the gate surface.[25] However, our ability to tune the IE of LPE-G enabled us to move the energetic level outside the band gap, as an alternative solution to introducing an additional dielectric interlayer. Our procedure permits to process from solution a conductive material that on the same time does not interact electronically with the active layer. This means that in a working regime where there are no percolation pathways across the LPE-G layer, the improved device performance must be attributed to the capacity of graphene to electrostatically charge upon the application of a gate potential, similarly to the case observed with reduced graphene oxide.[40] Graphene nanoflakes are able of carrying charges of both signs as revealed by the measurements done both with *n*- and *p*-type polymers. The electrostatic charging of the LPE-G nanopatches induces a higher amount of carriers within the measurement scan time frame leading to an enhanced device mobility regime for both polymers. In particular, the increase of performance is due to higher number of carriers between source-drain electrodes generated by appropriate gate voltage.

To prove our assumption we performed hysteresis measurements at different sweep times. First we tested pristine and enhanced semiconducting devices with double sweep measures as shown in Figure S18. Then we normalized curves obtained with respect to the highest I_{ds} current registered in order to evidence the differences in hysteresis windows as shown in Figure 5c. In pristine semiconductor mobility values show a discrepancy up to 15% when double sweep measures were performed, while V_{th} hysteresis shift is no more than 1 V for IIDDT-C3 and not more than 3 V for P(NDI2OD-T2). The shift is always in the opposite direction of the tracing curve. On the other hand, hysteresis behavior of devices with LPE-G on the SiO_2 surface is rather different. In the backward curves, P(NDI2OD-T2) devices with LPE-G nanopatches at the surface show a mobility increase up to 75% and V_{th} shift of at least 3.5 V (Figure 5a). Also IIDDT-C3/LPE-G based device show a marked hysteresis behavior: mobility is increased up to 60% of the original value when extracted from the backward curves, while V_{th} hysteresis window exceeds 15 V (Figure 5b). The current increases when gate voltage is inverted, indicating an accumulation of a surplus of carriers toward the drain happened in the first branch of the measure. The shortest is the sweeping time, the more pronounced is the hysteresis effect, proving very low charging time for graphene (complete analysis is given in the SI). Our results are in accordance with previous reports on P(NDI2OD-T2) featuring a low hysteresis.[41] On the same time normalized hysteresis measured in devices employing LPE-G on the gate surface polymers is markedly increased with respect to reference sample, demonstrating that the presence of graphene increases the number of carriers in the channel.

The devices presenting enhanced semiconducting behavior (II) were tested as memory device. Charges are accumulated in the floating LPE-G nanopatches and can be released upon applying a potential of opposite sign. Memory devices with reduced graphene oxide were already reported from solution casting,[42]

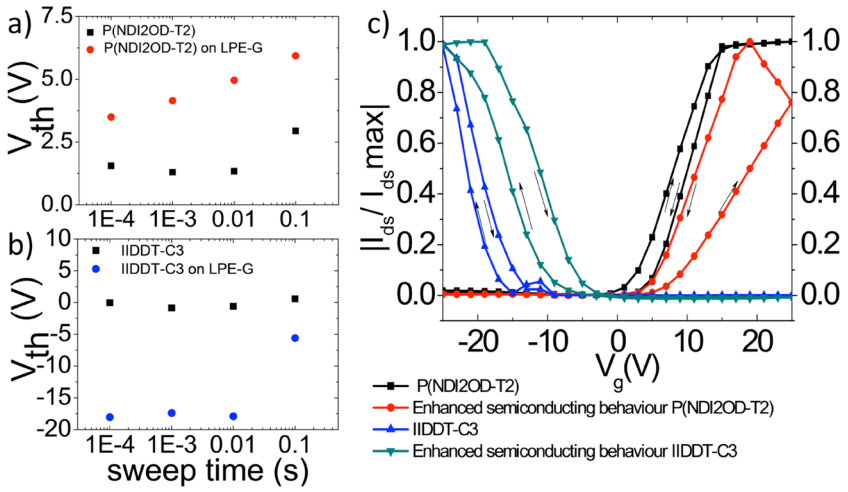

Figure 5. Threshold voltage (V_{th}) hysteresis shift between back and forth direction in different sweep time for (a) P(NDI2OD-T2) and (b) IIDDT-C3. (c) Hysteresis in the graphene patterned devices compared to pristine one for 0.1 s sweep time with respect to normalized I_{ds} current. Channel length 100 μm, width 10 000 μm, V_{ds} = 20 V for P(NDI2OD-T2) and V_{ds} = −20 V for IIDDT-C3.

patterned floating gate,[30] embedded in polymeric matrix,[43] by doping with gold[44] and to achieve multilevel resistive memory devices.[45] As aforementioned, our system exhibits two major advantages when compared to previously reported architectures of floating gate based OTFTs memory devices. In our study, LPE-G was employed for the first time for memory applications and it acts as charging layer without the need of an additional dielectric layer. This greatly simplifies the device fabrication while maximizing the effect of the electrostatic charges, which scales with the dielectric thickness. In addition, the floating gate density that gives rise to different device functioning regimes can be finely tuned by choosing a proper volume of LPE-G.

Both P(NDI2OD-T2)/LPE-G and IIDDT-C3/LPE-G enhanced devices were tested as memory device. When P(NDI2OD-T2)/LPE-G is used, a gate voltage of 60 V for 1 s was applied to write and a −60 V for 1 s to erase. When IIDDT-C3/LPE-G is employed, a gate voltage of −60 V for 1 s was applied to write and +100 V for 1 s to achieve the erase state. For the sake of comparison, the same cycles were performed on pristine polymer devices and no V_{th} shift was observed as reported in the SI.

P(NDI2OD-T2) memory devices display a V_{th} shift toward more positive values when the information is written, which led to a decrease of maximum current. The memory window is of about 5 V (Figure 6c). After applying a 1 s pulse with a gate voltage of opposite sign the transfer characteristic recorded moved back at the original position as shown in Figure 6a. All transfer characteristics were recorded at V_g = 40 V. Up to 50 writing/erasing cycles were performed in order to test the stability of the device as portrayed in Figure 6c. The hysteresis window remained constant all over the switching experiment with an initial small decrease. The retention time of the written state was also studied. The threshold voltage was found to be constant for the first 100 s; between 100 and 1000 s there is a small negative shift, and after 10^4 seconds the value is back at the starting position, as indicated with a blue dot line in Figure 6e. On the other hand, IIDDT-C3 memory device displays a threshold voltage shift toward more negative values when the programmed state is performed with a memory window of about 17 V. This high value is in agreement with hysteresis measurements, in which IIDDT-C3 shows a bigger shift with respect to P(NDI2OD-T2) TFTs (Figure 5a,b). After applying an opposite pulse of 100 V the transfer characteristic recorded moved back at the original position as illustrated in Figure 6b. All transfer characteristics were recorded at V_g = −40 V. As for the other based polymer 50 writing/erasing cycles were performed (Figure 6d). The memory window remained constant, programmed V_{th} values were very stable in both programmed and erased states and a difference of more 15 V was recorded after 50 cycles. Interestingly, the retention behavior is very similar to P(NDI2OD-T2). After applying the proper voltage to program a "writing" state the voltage shift was found being constant for the first 100 s, then a decrease was observed. Due to the higher memory window after 1000 s a shift value of over 10 V was still recorded. After this time a drastic positive shift toward the initial value was monitored (see Figure 6f). Overall, our results provide unambiguous confirmation of the electrostatic nature of the interaction between the two components. *Ad hoc* energetic alignment of the system under investigation enabled the LPE-G deposited and annealed to act as a floating gate; in other words, the graphene can be charged with an appropriate gate pulsed voltage. This led to the memory behavior, which exhibits interesting similarities with the hysteresis regime. In fact, as previously mentioned, the hysteresis windows is larger for IIDDT-C3 based TFTs with respect to P(NDI2OD-T2) and this is reflected by the larger V_{th} shift when a programmed cycles is performed on the former. From the memory

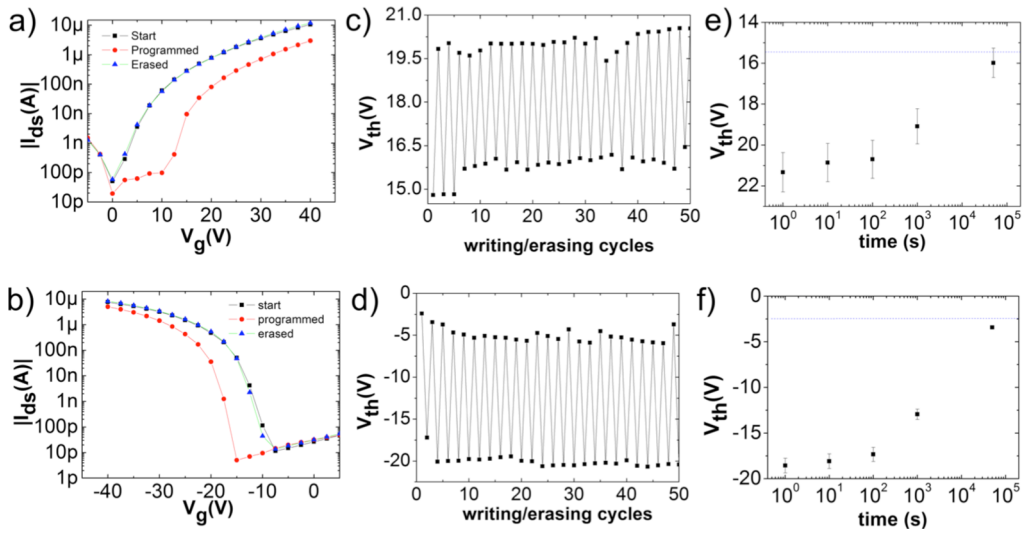

Figure 6. Transfer characteristic in log-scale of graphene enhanced devices in writing/erasing cycle for (a) P(NDI2OD-T2) and (b) IIDDT-C3. Writing was realized by applying a voltage pulse of −60 V to the gate electrode for 1 s for P(NDI2OD-T2) and 100 V for 1 s for IIDDT-C3. Erasing was achieved by applying a voltage pulse to the gate electrode for 1 s of 60 V P(NDI2OD-T2) and −60 V for 1 s for IIDDT-C3. V_{th} shift obtained by multiple of writing/erasing cycling for (c) P(NDI2OD-T2) and (d) IIDDT-C3. Retention time for programmed state of (e) P(NDI2OD-T2) and (f) IIDDT-C3. Initial V_{th} is reported by the dotted blue line. After applying a first appropriate voltage pulse, V_{th} was measured at different time up to when the value reached the initial one for both polymers. Retention time measurements displayed have been repeated three times. We report average values with their standard deviation.

windows values it was possible to roughly calculate the amount of charges stored in LPE-G using eq 1

$$\Delta V_{th} = \frac{Q}{C_i} \quad (1)$$

where C_i is the total capacitance, Q the stored charge in graphene flakes, and ΔV_{th} is the shift in threshold voltage. For our system we obtain a maximum value of surface charge amounting to 1.6×10^{12} cm^{-2} at $C_i = 15$ nF cm^{-2} when using IIDDT-C3, which is larger than the one previously reported (*cf.* ref 25). Since the LPE-G surface coverage is *ca.* 12% we can estimate also that the maximum number of accumulated charges would approach 1.3×10^{13} cm^{-2} on the assumption that the whole surface of SiO_2 is covered (full coverage).

The retention time measurement quantifies how long an information can be stored; *i.e.*, the device does not get discharged. The values of retention times which were obtained are slightly lower when compared to previous works where a dielectric layer between the floating gate and the semiconducting active channel is utilized.[30] The energy diagrams suggest that charges accumulated by electrostatic coupling (by the gate) on the LPE-G nanoflakes can be given to the semiconducting polymer. In addition, the fact that LPE-G at the gate dielectric surface enhances the charge transport suggests that predeposited LPE-G does not diffuse in the polymer matrix, a well-known effect[46] that is a major drawback for systems employing metallic nanoplates as floating gate.[25]

CONCLUSIONS

In summary, we devised a novel approach to fabricate a hybrid graphene-polymer thin-film transistor device whose electrical properties can be tuned for the first time *via* programming the ionization energy of one component upon highly reproducible thermal annealing treatments of the LPE-G preorganized on SiO_2 by solution processing. The engineered position of the LPE-G ionization energy was exploited to modulate the physics of transport within established polymeric semiconductors. Our approach was found to be of general applicability as it is proven with both electron and hole polymer semiconductors.

By exploiting the different electronic interactions between LPE-G and a polymer it was possible to devise the multifunctional PG-TFT operating simultaneously as a three-terminal and as a memory element. The conception of this device with a hybrid active material is only possible thanks to a fine combination and control over the peculiar starting properties of each single component. Applying the same concept with different materials, like patterning an organic/polymeric semiconductor with a certain IE may be possible but the deposition of a second solution-processable semiconductor on its top would alter dramatically the properties of the first polymer layer due to potential occurrence of phase segregation or dissolution. The PG-TFT was therefore fabricated taking advantage that LPE-G strongly physisorbs on the SiO_2 after annealing and it does not get dissolved in organic solvents.

Interestingly, the electronic performances of the PG-TFTs with the IE of the LPE-G lying outside the polymer gap were tuned by modifying the amount of LPE-G deposited into nanoflakes on the dielectric surface. Such a modulation made it possible not only to improve the mobility within the material, but also to

confer unique properties to the devices, including changing the mechanism of charge transport.

Furthermore, the crystallinity of the semiconducting polymer employed as active layer is unperturbed by the presence of the LPE-G, which is of paramount importance for technological exploitation. The electrostatic nature of the interaction and unique LPE-G properties were further exploited for the realization of a (flash) memory device without the need of an additional dielectric layer to separate the active polymer layer from the floating part. A number of interesting future developments can be foreseen using this new PG-TFTs strategy: while the easy deposition method qualifies this approach as a suitable large scale process for hybrid graphene/polymer device, the special memory effect arising from a controlled engineering of the LPE-G ionization energy paves the way for novel and exciting routes in materials science, soft matter physics and chemistry.

MATERIALS AND METHODS

LPE-G Exfoliation Procedure. In a typical exfoliation process, *N*-methyl-2-pyrrolidone (NMP) was purchased from Sigma-Aldrich and used as solvent for the exfoliation. Graphite powder (p.n. 332461) was also acquired from Sigma-Aldrich and used without further treatment. Graphene was prepared by liquid phase exfoliation as reported elsewhere.[5] Briefly, graphene dispersion was prepared by adding 100 mg of graphite powder in 10 mL of *N*-methyl-2-pyrrolidinone (NMP) (1 wt %) followed by bath ultrasonication (6 h) at 45 °C. Sonication of graphite powder led to gray liquid consisting of a homogeneous phase and large numbers of macroscopic aggregates, *i.e.*, unexfoliated graphitic material. These aggregates were removed by centrifugation (Eppendorf 5804, rotor F-34-6-38, 45 min at 10 000 rpm), yielding to a homogeneous dark dispersion. To quantify the concentration of graphene after centrifugation, a mixture of graphene dispersion and chloroform ($CHCl_3$) was first heated up to 50 °C for 30 min and then passed through polytetrafluoroethylene (PTFE) membrane filters (pore size 100 nm). The remaining solvent were washed several times with diethyl ether and $CHCl_3$. Careful measurements of the filtered mass were performed on a microbalance (Sartorius MSA2.75) to give the concentration of graphene after centrifugation. By analyzing 15 independent experiments, concentrations of graphene were obtained amounting 86 ± 10 μg mL^{-1}. Also the average lateral size of the LPE-graphene sheets was estimated to be 224 ± 50 nm and the percentage of mono- and bilayer thick flakes amounts to 16 ± 1%.

LPE-G Deposition on SiO_2. High quality thermally grown SiO_2 substrate ($n^{+2}Si/SiO_2$) (IPMS Fraunhofer) were cleaned by sonication in acetone and then isopropanol. They were carefully dried under nitrogen gas flow. Freshly LPE-G in NMP obtained as described above, was drop-casted on newly ozone treated (5 min irradiation +25 min incubation) $n^{+2}Si/SiO_2$ substrates. Samples were stored in a perfectly plane by spirit-level hoven for 4 h at 50 °C and then at 65 °C for other 2 h to allow gradual, partial solvent evaporation, letting graphene flakes to stick on the surface. Subsequently samples were annealed in air or in nitrogen atmosphere for 14 h at 415 °C to ensure complete solvent evaporation and removal of possible solvent residues.[47] Different amount of dispersions were drop-casted on samples, nominally [2.5:5:10:20] μL of LPE-G. LPE-G dispersion had a density of 86 μg/mL of graphene in NMP. To cover the whole surface (1.5×10^{-4} m^2 surface area) a minimum amount of 10 μL are necessary so for 2.5 and 5 μL we diluted the mother dispersion 4 and 2 times, respectively. Also blank samples was prepared with the same procedure, drop-casting 10 μL of pure NMP on samples and then providing thermal annealing at the same conditions of LPE-G samples, in order to have a reliable blank reference for TFTs electrical performance and behavior.

Device Preparation. LPE-G surface patterned Si-n^{+2}/SiO_2 samples were used as a scaffold for OTFTs device. In a cylindrical weighing bottle 38 μL of octadecyltrichlorosilane (purchased from Sigma-Aldrich, purity >90%, used with no further purification) were added to 10 mL of anhydrous toluene in nitrogen atmosphere. Selected samples were immersed in the solution which was then warmed for 30 min at 60 °C. Then the solution with the dipped samples was left reacting for 12 h. Samples were then rinsed with copious amount of toluene to ensure a complete cleaning, and then baked at 60 °C for 2 h. Solutions 5 mg/mL of P(NDI2OD-T2) and IIDDT-(C3) in chloroform were prepared and stirred overnight to ensure complete solubilization of the two polymers. 150 μL of polymer solution were spin-coated on the samples with different amount of deposited graphene on the surface. Reference samples were prepared too. For each polymer at least two sets of [0, 2.5, 5, 10, 15, 20] μL of deposited LPE-G were prepared. After spin coating the samples were annealed at 70° for 2 h to remove any solvent residual. Casted films were 60 nm thick for both polymers. As last step, 40 nm of gold were evaporated over the polymeric film to finalize top-contact, bottom gate devices. Each sample had 8 devices on it with channel length of 120, 100, 80, 60 μm and $W = 10\,000$ μm. P(NDI2OD-T2) OTFTs were then annealed for 14 h at 120 °C to avoid contact problem as reported in literature.[48]

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Deposited LPE-G optical microscope analysis, Deposited LPE-G SEM analysis, Deposited LPE-G thickness analysis by AFM, Parameter extraction, Devices output and transfer characteristics−electrical characterization, AFM morphology analysis of devices, structural characterization of P(NDI2OD-T2) and IIDDT-C3, LPE-G ambient photoelectron ionization potential spectroscopy, analysis of electrical hysteresis, XPS analysis. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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